Abstract

The present invention provides systems and methods for margin testing of one or more components of an electronic system, such as a computer system (e.g., a server). A margin testing system of the invention can include a fault bypass module incorporated in the electronic system for masking signals indicative of faults associated with one or more components during margin testing of the system. The margin testing system can also include a controller, such as a Baseboard Management Controller (BMC), internal to the electronic system that is in communication with the fault bypass module. The controller can transmit a command to the fault bypass module to initiate masking of selected faults by that module.

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